in each of said queues which prevents entries of memory or I/O transactions having low priority levels from using one of said queues before entries of memory or I/O transactions having higher priority levels.

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~~22.~~ A method according to Claim ~~18,~~ further comprising the step of determining priorities corresponding to entries of memory or I/O transactions by logical memory addresses, control bits derived from a memory management page table, control bits derived from segmentation entries, virtual addresses of a memory management system, programmable registers which set priorities for each processor, instructions, or instruction operands.--

REMARKS

Prior to the examination of the above-identified U.S. patent application, please enter the following preliminary amendments. The title of the application has been changed to better describe the application. Claims 21 and 22 have been added. The addition of these claims do not add new matter and is fully supported in the specification attached herewith.

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Applicants believe that the application as filed is fully in condition for allowance, and early notification of such is hereby earnestly requested.

Respectfully submitted,

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